

a request of a user or according to an internal management policy (e.g., a power consumption policy, an attack defense policy, or the like) of the mobile device **2000**.

[0140] The processor **2100** may be configured to control an overall operation of the mobile device **2000** and a wired/wireless communication between the mobile device **2000** and an external device. For example, the processor **2100** may be an application processor (AP), an integrated modem application processor (hereinafter referred to as “ModAP”), a microprocessor or the like.

[0141] The buffer memory **2200** may be configured to temporarily store data, which is used when the mobile device **2000** performs a process operation. The display/touch module **2300** may be configured to display data processed from the processor **2100** or to receive data from a touch panel. The storage device **2400** may be configured to store data of a user. The storage device **2400** may be eMMC, SSD, UFS, or the like.

[0142] FIG. **18** is a graph exemplarily illustrating an operating result of a glitch detector according to an exemplary embodiment. Referring to FIG. **18**, a glitch detector according to an exemplary embodiment may detect a positive glitch which varies suddenly high and a positive glitch which varies smoothly, as well as a negative glitch. Here, the positive glitch may denote the time when a moving average is greater than upper limit, and the negative glitch may denote the time when the moving average is smaller than lower limit.

[0143] In some exemplary embodiments, the upper limit and the lower limit may be fixed. In some exemplary embodiments, an external system may change the upper limit and/or the lower limit using software. That is, a sensitivity of a glitch detector may be adjustable.

[0144] According to exemplary embodiments, a glitch detector, an electronic device having the same, and an alarm signal generating method thereof may detect a glitch using digital circuits, thereby reducing the size of the glitch detector, comparing to an analog circuit, and making it possible to apply various semiconductor processes without modification.

[0145] Furthermore, according to exemplary embodiments, a glitch detector, an electronic device having the same, and an alarm signal generating method may change a reference value in various operating environments, thereby adjusting a sensitivity of the glitch detector.

[0146] While the inventive concept has been described with reference to exemplary embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present inventive concept. Therefore, it should be understood that the above exemplary embodiments are not limiting, but illustrative.

1. A glitch detector comprising:

- a clock generator configured to generate a clock corresponding to a power voltage;
- a counter configured to count the clock generated by the clock generator and to output a count value; and
- a comparator configured to compare a reference value with the count value output by the counter and to generate an alarm signal based on a result of the comparison.

2. The glitch detector of claim 1, wherein the clock generator comprises a ring oscillator.

3. The glitch detector of claim 1, wherein the counter comprises a ripple counter.

4. The glitch detector of claim 1, further comprising a synchronizer configured to synchronize the count value with a system clock that is different from the clock generated by the clock generator.

5. The glitch detector of claim 4, wherein the count value output by the counter is a binary code value,

the glitch detector further comprising:

- a binary gray code converter configured to convert the binary code value into a gray code value and to output the converted gray code value to the synchronizer, the synchronizer being configured to synchronize the converted gray code value with the system clock, and
- a gray code converter configured to convert the synchronized gray code value into a binary code value and to output the converted binary code value to the comparator.

6. The glitch detector of claim 1, further comprising a reference value generator configured to generate the reference value.

7. The glitch detector of claim 6, wherein the reference value is a fixed value.

8. The glitch detector of claim 6, wherein the reference value is a variable value.

9. The glitch detector of claim 8, wherein the reference value is a moving average value.

10. The glitch detector of claim 9, wherein the comparator is configured to generate the alarm signal when an absolute value of the count value minus the moving average value is greater than a threshold value.

11. The glitch detector of claim 9, wherein the comparator is configured to generate the alarm signal when the count value is greater than the moving average value, and the count value is greater than an upper limit, or

wherein the comparator is configured to generate the alarm signal when the count value is not greater than the moving average value, and the count value is less than a lower limit.

12. The glitch detector of claim 8, wherein the reference value is a prior count value, and

wherein the comparator is configured to generate the alarm signal when an absolute value of the count value minus the prior count value is greater than a threshold value.

13. The glitch detector of claim 8, wherein the comparator is configured to generate the alarm signal when the count value is greater than an upper limit, or

wherein the comparator is configured to generate the alarm signal when the count value is not greater than the upper limit, and the count value is less than a lower limit.

14. The glitch detector of claim 1, wherein the clock generator is configured to generate the clock in a counting section of a system clock domain, and to not generate the clock in a transferring section of the system clock domain, and

wherein the counter is configured to count the clock in the counting section of the system clock domain, and to output the count value to the comparator in the transferring section of the system clock domain.